CMOS Dual Complementary Pair Plus Inverter

High-Voltage Types (20-Volt Rating)

- CD4007UB types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Fig. 2.

More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007UB types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Applications:
- Extremely high-input impedance amplifiers
- Shapers
- Inverters
- Threshold detector
- Linear amplifiers
- Crystal oscillators

**Features:**
- Standardized symmetrical output characteristics
- Medium Speed Operation \( t_{PHL}, t_{PLH} \approx 30 \text{ ns (typ.)} \) at 10 V
- 100% tested for quiescent current at 20 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Maximum input current of 1 \( \mu \text{A} \) at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

**RECOMMENDED OPERATING CONDITIONS**
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply-Voltage Range (For ( T_A = \text{Full Package Temperature Range} ))</td>
<td>3 18</td>
<td>V</td>
</tr>
</tbody>
</table>

**STATIC ELECTRICAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>CONDITIONS</th>
<th>LIMITS AT INDICATED TEMPERATURES (°C)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(O) (V)</td>
<td>V(IN) (V)</td>
<td>V(DD) (V)</td>
<td>( -55 )</td>
</tr>
<tr>
<td>Quiescent Device Current, ( I_{DD , \text{Max.}} )</td>
<td>(-)</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Output Low (Sink) Current, ( I_{OL , \text{Min.}} )</td>
<td>0.5</td>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>Output High (Source) Current, ( I_{OH , \text{Min.}} )</td>
<td>1.5</td>
<td>0.15</td>
<td>15</td>
</tr>
<tr>
<td>Output Voltage: Low-Level, ( V(O) , \text{Max.} )</td>
<td>(-)</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Input Voltage, ( \text{High-Level} ), ( V(IH , \text{Min.}} )</td>
<td>(-)</td>
<td>0.15</td>
<td>15</td>
</tr>
<tr>
<td>Input Current, ( I_{IH , \text{Max.}} )</td>
<td>0.18</td>
<td>18</td>
<td>( \pm 0.1 )</td>
</tr>
</tbody>
</table>

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MAXIMUM RATINGS, Absolute-Maximum Values:
DC SUPPLY-VOLTAGE RANGE, (VDD)
  Voltages referenced to VSS Terminal) .................................... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ........................................... -0.5V to VDD +0.5V
DC INPUT CURRENT, ANY ONE INPUT ......................................... ±10mA
POWER DISSIPATION PER PACKAGE (PD):
  For TA = -55°C to +100°C ...................................................... 500mW
  For TA = +100°C to +125°C .................................................... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ......... 100mW
OPERATING-TEMPERATURE RANGE (TA) ........................................... -55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg) ......................................... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ...................... +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at TA = 25°C; Input tr, tf = 20 ns,
C L = 50 pF, R L = 200 KΩ

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>CONDITIONS</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD Volts</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Propagation Delay Time:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>τPHL, τPLH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>55</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>10</td>
<td>30</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>25</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Transition Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>τTHL, τTLH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>100</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>10</td>
<td>50</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>40</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Any Input</td>
<td>10</td>
<td>15</td>
</tr>
</tbody>
</table>

Fig. 1 – Detailed schematic diagram of CD4007UB showing input, output, and parasitic diodes.

Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB.
CD4007UB Types

e) High Sink-Current Driver

f) High Source-Current Driver

(6,3,10); (8,5, 12); (11,14); (7,4,9)

(6,3,10); (13,1,12); (14,2,11); (7,9)

h) Dual Bi-Directional Transmission Gating

(1,5,12); (2,9); (11,4); (8,13,10); (6,3)

Fig. 2 – Sample CMOS logic circuit arrangements using type CD4007UB (Cont’d).

Fig. 3 – Typical voltage-transfer characteristics for NAND gate.

Fig. 4 – Typical voltage-transfer characteristics for NOR gate.

Fig. 5 – Minimum output low (sink) current characteristics.

Fig. 6 – Minimum and maximum voltage-transfer characteristics for inverter.

Fig. 7 – Typical current and voltage-transfer characteristics for inverter.

Fig. 8 – Minimum output low (sink) current characteristics.
CD4007UB Types

Fig. 9 — Typical output high (source) current characteristics.

Fig. 10 — Minimum output high source current characteristics.

Fig. 11 — Typical voltage-transfer characteristics as a function of temperature.

Fig. 12 — Typical propagation delay time vs. load capacitance.

Fig. 13 — Typical transition time vs. load capacitance.

Fig. 14 — Typical dissipation vs. frequency characteristics.

Fig. 15 — Input current test circuit.

Fig. 16 — Input voltage test circuit.

Fig. 17 — Quiescent device current test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^-3 inch).

50–56
(1.270–1.473)

54–62
(1.372–1.574)

4–10
(0.102–0.254)

DIMENSIONS AND PAD LAYOUT FOR CD4007UBH

3-17
CERAMIC DUAL IN-LINE PACKAGE

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td></td>
<td>BSC</td>
<td>BSC</td>
<td>BSC</td>
<td>BSC</td>
</tr>
<tr>
<td>B MAX</td>
<td>0.785 (19.94)</td>
<td>0.840 (21.34)</td>
<td>0.960 (24.38)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>B MIN</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>C MAX</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.310 (7.87)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td>C MIN</td>
<td>0.245 (6.22)</td>
<td>0.245 (6.22)</td>
<td>0.220 (5.59)</td>
<td>0.245 (6.22)</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

4040083/F 03/03
NOTES:

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
D (R-PDSO-G**)  
PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

**NOTES:**
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0.15).
D. Falls within JEDEC MS-012
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
MECHANICAL DATA

PW (R-PDSO-G**)  PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-153
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